

# ASCON

(A Submission to CAESAR)

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# Overview

- CAESAR
- Design of Ascon
- Security analysis
- Implementations

# CAESAR

- CAESAR: Competition for Authenticated Encryption – Security, Applicability, and Robustness (2014–2018)
  - <http://competitions.cr.yp.to/caesar.html>
  - Inspired by AES, eStream, SHA-3
- Authenticated Encryption
  - Confidentiality as provided by block cipher modes
  - Authenticity, Integrity as provided by MACs

*"it is very easy to accidentally combine secure encryption schemes with secure MACs and still get insecure authenticated encryption schemes"*

– Kohno, Whiting, and Viega

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# Generic compositions

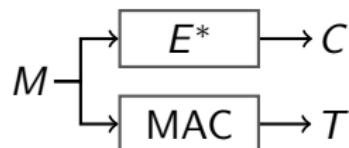
## MAC-then-Encrypt (MtE)

- e.g. in SSL/TLS
- security depends on  $E$  and MAC



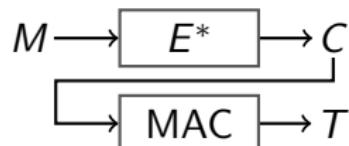
## Encrypt-and-MAC (E&M)

- e.g. in SSH
- security depends on  $E$  and MAC



## Encrypt-then-MAC (EtM)

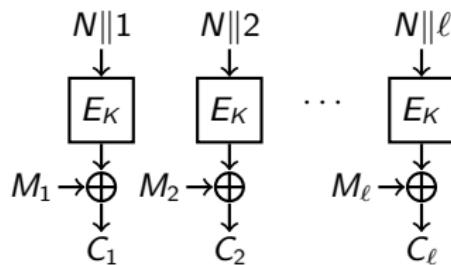
- IPSec, ISO/IEC 19772:2009
- provably secure



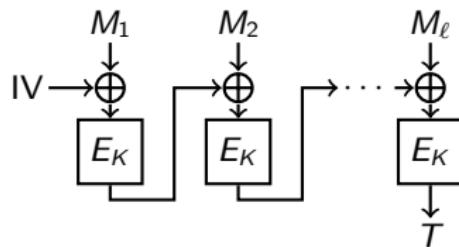
# Pitfalls: Dependent Keys (Confidentiality)

Encrypt-and-MAC with CBC-MAC and CTR

CTR



CBC-MAC

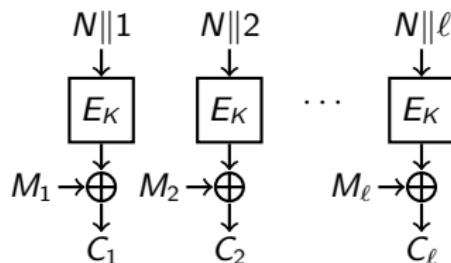


What can an attacker do?

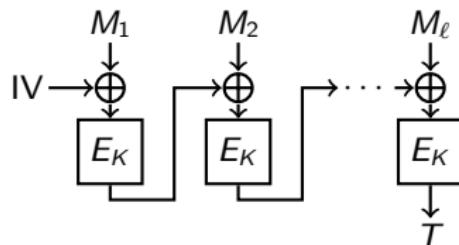
# Pitfalls: Dependent Keys (Confidentiality)

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CBC-MAC



What can an attacker do?

Tags for  $M = IV \oplus (N\|1)$ ,  $M = IV \oplus (N\|2)$ , ...  
are the key stream to read  $M_1, M_2, \dots$

(Keys for)  $E^*$  and MAC must be independent!

# CAESAR – Candidates

ACORN	++AE	AEGIS	AES-CMCC
AES-COBRA	AES-COPA	AES-CPFB	AES-JAMBU
AES-OTR	AEZ	Artemia	Ascon
AVALANCHE	Calico	CBA	CBEAM
CLOC	Deoxys	ELmD	Enchilada
FASER	HKC	HS1-SIV	ICEPOLE
iFeed[AES]	Joltik	Julius	Ketje
Keyak	KIASU	LAC	Marble
McMambo	Minalpher	MORUS	NORX
OCB	OMD	PAEQ	PAES
PANDA	$\pi$ -Cipher	POET	POLAWIS
PRIMATEs	Prøst	Raviyoyla	Sablier
SCREAM	SHELL	SILC	Silver
STRIBOB	Tiaoxin	TriviA-ck	Wheesht
YAES			

# CAESAR – Candidates

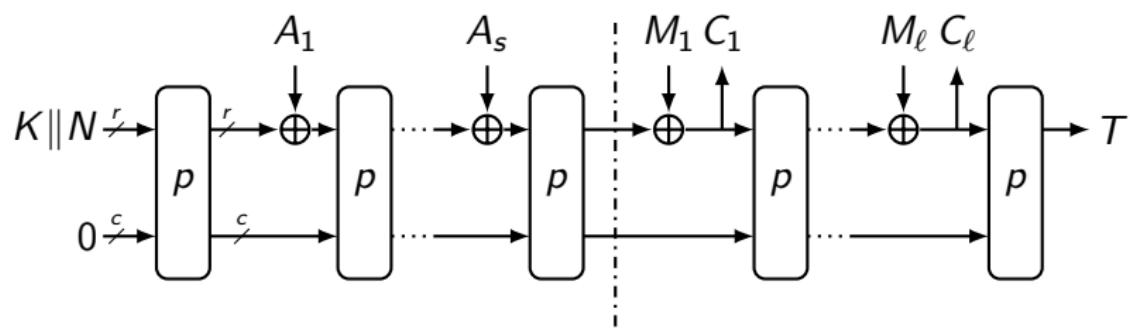
ACORN	<del>+AE</del>	AEGIS	<del>AES-CMCC</del>
<del>AES-COBRA</del>	AES-COPA	<del>AES-CPFB</del>	AES-JAMBU
AES-OTR	AEZ	<del>Artemia</del>	<a href="#">Ascon</a>
<del>AVALANCHE</del>	<del>Calico</del>	<del>CBA</del>	<del>CBEAM</del>
CLOC	Deoxys	ElmD	<del>Enchilada</del>
<del>FASER</del>	<del>HKC</del>	HS1-SIV	ICEPOLE
iFeed[AES]	Joltik	<del>Julius</del>	Ketje
Keyak	<del>KIASU</del>	<del>LAC</del>	<del>Marble</del>
McMambo	Minalpher	MORUS	NORX
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<del>YAES</del>			

# ASCON – Design Goals

- Security
- Efficiency
- Lightweight
- Simplicity
- Online
- Single pass
- Scalability
- Side-Channel robustness

## Duplex sponge constructions

- Sponges became popular with SHA-3 winner Keccak
- Can be transformed to AE mode: duplex sponges
- Based on permutation  $p$  instead of block cipher  $E_K$
- Security parameter: capacity  $c$

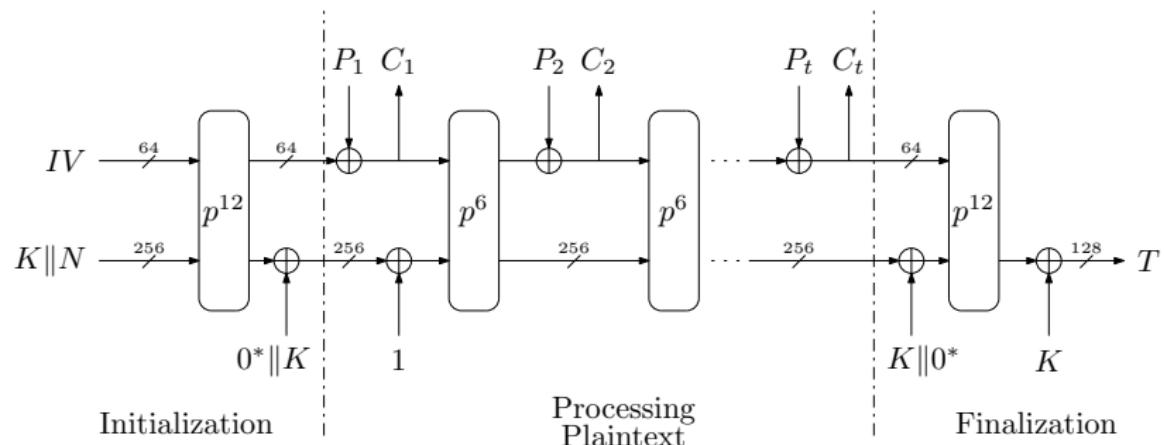


# ASCON – General Overview

- Nonce-based AEAD scheme
- Sponge inspired

ASCON-128:  $(c, r) = (256, 64)$

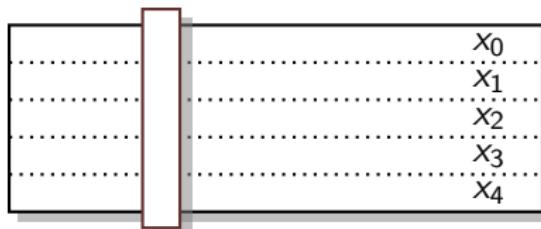
ASCON-96:  $(c, r) = (192, 128)$



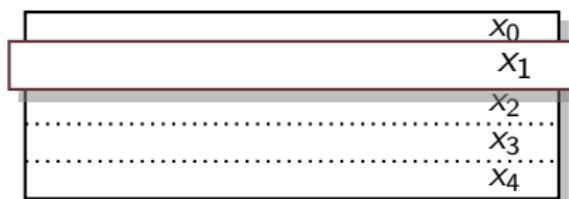
# Ascon – Permutation

320-bit permutation, several rounds of:

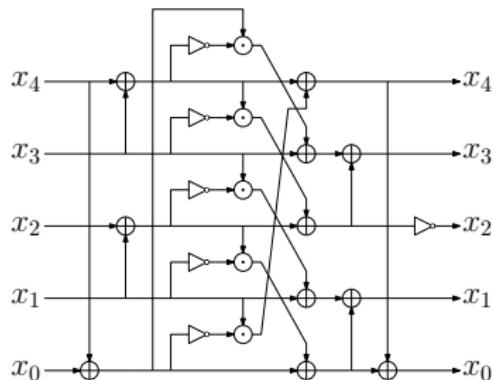
- Constant addition
- S-Box layer



- Linear transformation



# ASCON – Round



S-box

$$x_4 \oplus (x_4 \ggg 7) \oplus (x_4 \ggg 41) \rightarrow x_4$$

$$x_3 \oplus (x_3 \ggg 10) \oplus (x_3 \ggg 17) \rightarrow x_3$$

$$x_2 \oplus (x_2 \ggg 1) \oplus (x_2 \ggg 6) \rightarrow x_2$$

$$x_1 \oplus (x_1 \ggg 61) \oplus (x_1 \ggg 39) \rightarrow x_1$$

$$x_0 \oplus (x_0 \ggg 19) \oplus (x_0 \ggg 28) \rightarrow x_0$$

Linear transformation

## Analysis – Permutation

- Branch number 3 for S-box and linear transformation
- Proof on minimum number of active S-boxes
- Search for differential and linear characteristics

result	rounds	differential	linear
proof	1	1	1
	2	4	4
	3	15	13
heuristic	4	44	43
	$\geq 5$	$> 64$	$> 64$

# Analysis – ASCON [DEMS15]

- Analysis of the building blocks
  - Permutation
- Attacks on round-reduced versions of ASCON-128
  - Key-recovery
  - Forgery

	rounds	time	method
ASCON-128	6 / 12	$2^{66}$	cube-like
	5 / 12	$2^{35}$	
	5 / 12	$2^{36}$	differential-linear
	4 / 12	$2^{18}$	

# Implementation – ASCON

- Software
  - 64-bit Intel platforms
  - ARM NEON
  - 8-bit ATmega128
- Hardware [GWDE15]
  - High-speed
  - Low-area
  - Threshold implementations

## Software – 64-bit Intel

- One message per core (Core2Duo)

	64	512	1024	4096
ASCON-128 (c/B)	22.0	15.9	15.6	15.2
ASCON-96 (c/B)	17.7	11.0	10.5	10.3

- Four messages per core [Sen15] (Haswell)

	64	512	1024	4096
ASCON-128 (c/B)	10.49	7.33	7.11	6.94
ASCON-96 (c/B)	8.55	5.26	5.02	4.85

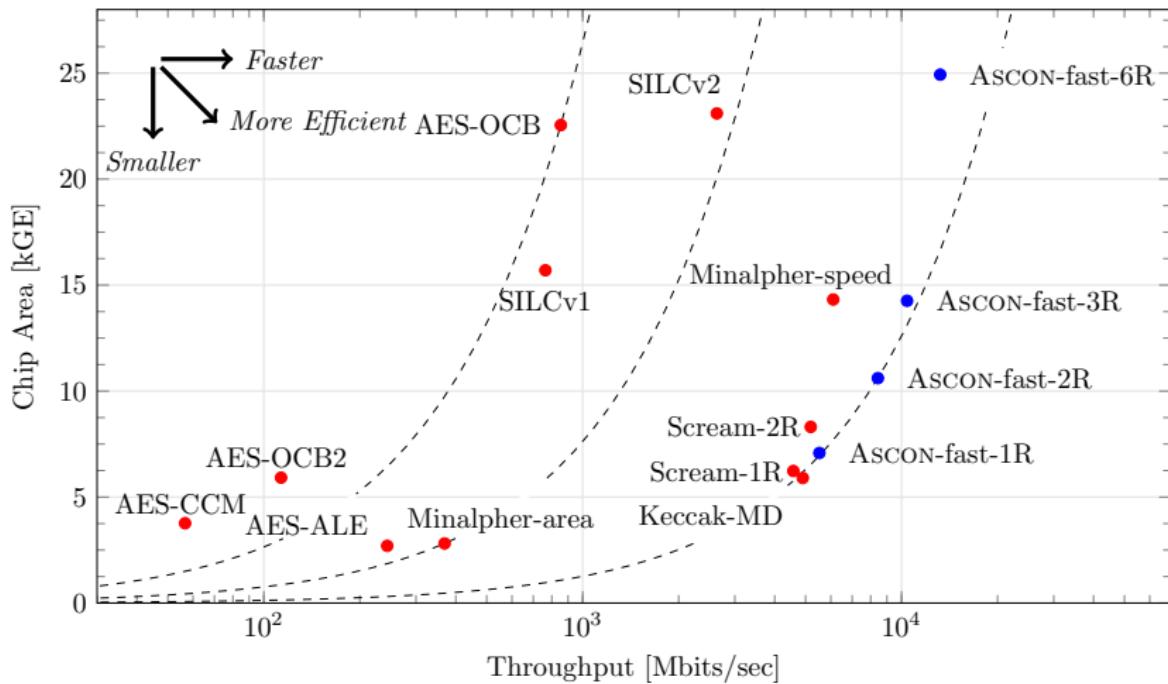
## Hardware – Results [GWDE15]

	Chip Area [kGE]	Throughput [Mbps]	Power [µW]	Energy [µJ/byte]
<b>Unprotected Implementations</b>				
Fast 1 round	7.08	5 524	43	33
Fast 6 rounds	24.93	13 218	184	23
Low-area	2.57	14	15	5 706

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<b>Threshold Implementations</b>				
Fast 1 round	28.61	3 774	183	137
Fast 6 rounds	123.52	9 018	830	104
Low-area	7.97	15	45	17 234

# Hardware – Comparison [GWDE15]



## Ascon-128 – Choice of Parameters

- Now:  $(c, r) = (256, 64)$ 
  - Conservative choice
- Proposed:  $(c, r) = (192, 128)$  [BDPA11]
  - Significant speedup (factor 2)
  - Limit on data complexity  $2^{64}$
- Proposed:  $(c, r) = (128, 192)$  [JLM14]
  - Significant speedup (factor 3)
  - More analysis needed

## More Information

<http://ascon.iaik.tugraz.at>

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